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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,240	03/31/2004	Masashi Horiguchi	500.28006C10	4827

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,240	HORIGUCHI ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/818,434.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/31/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: search history.

DETAILED ACTION

Information Disclosure Statement

1. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 31 March 2004. The information disclosed therein was considered.

Specification

2. The disclosure is objected to because of the following informalities:

The status of the parent application No. 10/401,975 should be updated; namely, said application has matured into U.S. Pat. No. 6,754,114.

Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,617,365 ("Reference").

Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claims 1 and 3-11 of Application are anticipated by claim 1 of Reference, since claim 1 of Reference recites memory mats ("a first memory mat and a second memory mat" in claim 1 of Reference) each formed with word lines, bit lines, a spare bit line ("a first spare bit line" in claim 1 of Reference), and memory cells (inherent); a spare bit line selection line ("a first spare bit line selection line" in claim 1 of Reference) coupled to the memory mats, wherein the respective spare bit lines in the memory mats are selected when said spare bit line selection line is activated (as implied by "a spare bit line selection circuit...selecting said first spare bit line" in claim 1 of Reference); a pair of comparison circuits, or a first comparison circuit and a second comparison circuit, or comparison means, or redundancy control means, or a redundancy circuit ("a first address comparing circuit" and "a second address comparing circuit" in claim 1 of Reference), each formed with memory means (as implied by a defective address being "stored therein" in claim 1 of Reference) and an output coupled to said spare bit lines selection line (via the "first logical OR gate" in claim 1 of Reference), the memory means of said first comparison circuit being stored with a first defect information ("a first defective address" in claim 1 of Reference) associated with a first defect in a first defect mode, as recited in claims 1 and 3-11 of Application, and the memory means of said second comparison circuit being stored with a second defect information ("a second defective address" in claim 1 of Reference) associated with a second defect in a second defect mode, wherein each comparing each comparing circuit compares the defect information (the "defective address" in claim 1 of Reference) with input signals including address signals ("a portion of an access address" in claim 1 of Reference)

indicative of selections of the memory mats ("a part of row address" in claim 1 of Reference) and indicative of selections of the bit line selection lines ("a column address" in claim 1 of Reference), as recited in claims 1 and 3-11 of Application. However, claim 1 of Reference does not disclose a plurality of bit selection lines, as recited in claim 1 and 3-11 of Application. In view of claim 1 of Reference reciting the spare bit selection line as in claims 1 and 3-11 of Application, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate a plurality of bit line selection lines coupled to the memory mats, such that respective ones of the bit lines in the memory mats are selected when one of bit line selection lines is activated, as recited in claims 1 and 3-11 of Application, to complement and parallel the structure and operation of the spare bit line selection line for accessing of memory cells without defects.

Claim 2 of Application is anticipated also by claim 1 of Reference, since claim 1 of Reference recites an OR circuit ("a first logical OR gate" in claim 1 of Reference) having inputs coupled to outputs of said pair of comparison circuits ("a first address comparing circuit" and "a second address comparing circuit" in claim 1 of Reference) and an output coupled to said spare bit line selection line.

5. Claims 12-21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 7 of U.S. Patent No. 6,104,647 ("Reference"). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claims 12, 14-16, 18, 19 and 21 of Application are anticipated by claim 1 of Reference, since claim 1 of Reference recites memory mats each having word lines, bit lines, a spare bit line and memory cells; bit lines selection lines; a spare bit selection line; a redundancy circuit; programmable means or memory means ("programmable elements" in claim 1 of Reference which can be programmed for one of a first defect mode and a second mode, implying the programmable elements would store defective information); a first defect mode associated with a first defect so as to activate the spare bit line selection line depending on an access to one of memory mats, and a second defect mode associated with a second defect so as to activate said spare bit line selection line depending on an access of any one of memory mats. However, claim 1 of Reference does not recite an associated method of manufacturing such a memory device comprising the steps of preparing a semiconductor ship formed with the elements recited in claim 1 of Reference. In view of claim 1 of Reference, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to manufacture the memory device of claim 1 of Reference using the steps recited in claims 12, 14-16, 18, 19 or 21 of Application, since it was well known in the art to manufacture a memory device, such as that recited in claim 1 of Reference, with the steps of preparing semiconductor chip with the elements recited in claim 1 of Reference, and programming the memory means or the programmable means in accordance with a defect found on the semiconductor chip, as recited in claims 12, 14-16, 18, 19 or 21 of Application.

Claims 13, 17 and 20 of Application are anticipated by claim 7 of Reference, since claim 7 recites that each of the programmable elements of claim 1 of Reference is a fuse, which are inherently programmable, and, in the above programming step of claims 12, 14-16, 18, 19 or 21

of Application, it would inherently require cutting off the fuse correspondingly to the defect found on said semiconductor chip.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Furutani et al. (U.S. Pat. No. 4,849,938) discloses a memory with a redundancy configuration having a line of spare memory cells and an address comparison circuit.

Nanbu et al. (U.S. Pat. No. 4,733,372) discloses a memory with redundancy having a spare memory and an address comparison circuit.

Horiguchi et al. (U.S. Pat. No. 6,754,114) is a patent associated with a parent application of the instant application.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

RICHARD ELMS
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